MEMORY SYSTEM WITH REDUCED REFRESH CURRENT

Abstract

The present invention is a random access memory device with reduced refresh current and method for use in the same. The memory device includes a memory array with a plurality of memory cells. The memory cells are configured to hold a charge. A command block is coupled to the memory bank and is configured to receive refresh commands that are used to periodically refresh the memory cells. A detection circuit is coupled to the command block and to the memory array. The detection circuit is configured to store a hit detect signal when the memory array is accessed. The detection circuit also receives the refresh command. The detections circuit enables block select signals only when the hit detect signal is stored while the refresh command is received.